## REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed February 25, 2005 (Paper No. 1). Upon entry of this response, claims 1-8, 10-17, 19-25, 33-46, and 61-90 are pending in the application. In this response, Applicants have amended claim 19, cancelled claims 9, 18, 26-32 and 47-60, and added new claims 68-90. Applicants respectfully request that the amendments being filed herewith be entered and request that there be reconsideration of all pending claims.

1. Specification Amendments

Applicants respectfully assert that the amendments made to the specification herein do not add new matter. Support for the amendments can be found at least in the first two full paragraphs on p. 6 of the provisional (Serial No. 60/208,639) to which the instant application claims priority.

2. Rejection of Claims 1-67 under 35 U.S.C. §103

Claims 1-67 have been rejected under §103(a) as allegedly obvious over *Delvaux* (U.S. 6,718,419) in view of *Delattre et al.* (U.S. 6,606,302). Applicants respectfully traverse these rejections. It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly, all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical*, 5 U.S.P.Q. 2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

a. Claim 1

Applicants respectfully traverse the rejection of claim 1, and submit that claim 1 is allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the following features.

1) The proposed combination does not disclose, teach, or suggest "each of the plurality of physical layer devices having a first channel port associated with the first class of service and a second channel port associated with the second class of service"

The Office Action alleges that "*Delvaux* discloses two ports (see fig 8) for each physical layer device." (Office Action, p. 2.) Applicants respectfully disagree, and submit that Fig. 8 shows merely that each physical layer device has ***two sets of input lines*** which together form a standard UTOPIA 5 bit address: range line 165 selects one set of four PHYs, while address bus 169 provides the least significant 4 address bits to each PHY. Applicants further submit that to one skilled in the art, an address line is not equivalent to a port. Rather, a port is an addressable entity within a device. Ports have addresses, but addresses are not ports.

The Office Action also alleges that "*Delattre et al.* discloses a number of shapers (defined by class of service, VBR and ABR) dedicated for their respective ports (see fig 5a and Col 9 lines 40-59)." (Office Action, p. 2.) Applicants respectfully disagree. The shapers in *Delattre et al.* are not dedicated to one port. *Delattre et al.* discloses instead that a shaper is associated with a "tree," and that "a shaper processes the cells of all the point-to-multipoint connections associated with the tree." (Col. 9, lines 20-25.) Other passages in *Delattre et al.* explain that a "tree" is "constituted by the data element of its input line card (root) and its output ports (leaves)." (Col. 9, lines 10-15.) Thus, *Delattre et al.* teaches that a shaper is associated with ***multiple ports***.

2) The proposed combination does not disclose, teach, or suggest "wherein at least two of the plurality of channel connections associated with the plurality of first channel ports is via no more than one of the plurality of addresses"

Even assuming, *arguendo*, that the proposed combination discloses physical layer devices (PHYs) having two ports, *Delvaux* does not disclose the manner in which these ports are used to establish channel connections. In Applicants' claimed invention, as defined by claim 1, a single address ("no more than one of the plurality of addresses") is used to establish more than one channel connection. Furthermore, the channel connections established through this single address are associated with one specific port on each PHY ("first channel ports"). These features are not disclosed, taught, or suggested by *Delvaux* or by *Delattre et al.*

3) Conclusion

Accordingly, the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 1. Since the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 1, a *prima facie* case establishing an obviousness rejection by *Delvaux* in view of *Delattre et al.* has not been made. Thus, claim 1 is not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

b. Claim 10

Applicants respectfully traverse the rejection of claim 10, and submit that claim 10 is allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the following features.

1) The proposed combination does not disclose, teach, or suggest "each of the plurality of physical layer devices having a first channel port associated with the first class of service and a second channel port associated with the second class of service"

The Office Action alleges that "*Delvaux* discloses two ports (see fig 8) for each physical layer device." (Office Action, p. 4.) Applicants respectfully disagree, and submit that Fig. 8 shows merely that each physical layer device has ***two sets of input lines*** which together form a standard UTOPIA 5 bit address: range line 165 selects one set of four PHYs, while address bus 169 provides the least significant 4 address bits to each PHY. Applicants further submit that to one skilled in the art, an address line is not equivalent to a port. Rather, a port is an addressable entity within a device. Ports have addresses, but addresses are not ports.

The Office Action also alleges that "*Delattre et al.* discloses a number of shapers (defined by class of service, VBR and ABR) dedicated for their respective ports (see fig 5a and Col 9 lines 40-59)." (Office Action, p. 5.) Applicants respectfully disagree. The shapers in *Delattre et al.* are not dedicated to one port. *Delattre et al.* discloses instead that a shaper is associated with a "tree," and that "a shaper processes the cells of all the point-to-multipoint connections associated with the tree." (Col. 9, lines 20-25.) Other passages in *Delattre et al.* explain that a "tree" is "constituted by the data element of its input line card (root) and its output ports (leaves)." (Col. 9, lines 10-15.) Thus, *Delattre et al.* teaches that a shaper is associated with ***multiple ports***.

2) The proposed combination does not disclose, teach, or suggest "each of the first plurality of channel connections via one of a portion of a plurality of addresses associated with the first local interface; an address expansion device in communication with the first local interface via the remaining portion of the plurality of addresses"

*Delvaux* discloses a bus 161 ("first local interface") between the ATM layer device and multiple physical layer devices (PHYs), and an address extension device 160 ("address

expansion device") connected to bus 161. Given a 6-bit device address, the address expansion device 160 operates as follows. Range select decoder 162 uses the two most significant bits to select one of 4 groups of PHYs. The 4 least significant bits are passed through to the selected PHY group. Thus, the 6-bit input address is condensed to a 5-bit address that is supplied to each PHY. The address extension device 160 operates as a pass-through for addresses on bus 161, but does not itself have an address on bus 161.

In contrast, Applicants' claimed invention as defined in claim 10 divides local interface addresses into two portions. One portion is used to establish connections to the physical layer devices. The "remaining portion" is used by the address expansion device. These features are not disclosed, taught, or suggested by *Delvaux* or by *Delattre et al.*

3) Conclusion

Accordingly, the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 10. Since the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 10, a *prima facie* case establishing an obviousness rejection by *Delvaux* in view of *Delattre et al.* has not been made. Thus, claim 10 is not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

c. Claim 19

Applicants respectfully submit that the rejection of claim 19 has been overcome by the amendments made herein. Applicants respectfully submit that amended claim 19 is allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the following features.

1) The proposed combination does not disclose, teach, or suggest "each of the plurality of physical layer devices having a first port associated with the first class of service and a second port associated with the second class of service"

*Delvaux* does not disclose two ports for each physical layer device. *Delvaux* (Fig. 8) shows merely that each physical layer device has ***two sets of input lines*** which together form a standard UTOPIA 5 bit address: range line 165 selects one set of four PHYs, while address bus 169 provides the least significant 4 address bits to each PHY. Applicants further submit that to one skilled in the art, an address line is not equivalent to a port. Rather, a port is an addressable entity within a device. Ports have addresses, but addresses are not ports.

The Office Action also alleges that "*Delattre et al.* discloses a number of shapers (defined by class of service, VBR and ABR) dedicated for their respective ports (see fig 5a and Col 9 lines 40-59)." (Office Action, p. 7.) Applicants respectfully disagree. The shapers in *Delattre et al.* are not dedicated to one port. *Delattre et al.* discloses instead that a shaper is associated with a "tree," and that "a shaper processes the cells of all the point-to-multipoint connections associated with the tree." (Col. 9, lines 20-25.) Other passages in *Delattre et al.* explain that a "tree" is "constituted by the data element of its input line card (root) and its output ports (leaves)." (Col. 9, lines 10-15.) Thus, *Delattre et al.* teaches that a shaper is associated with ***multiple ports***.

2) The proposed combination does not disclose, teach, or suggest "wherein at least two of the plurality of channel connections associated with the plurality of first ports is via no more than one of the plurality of addresses"

Even assuming, *arguendo*, that the proposed combination discloses physical layer devices (PHYs) having two ports, *Delvaux* does not disclose the manner in which these ports are used to establish channel connections. In Applicants' claimed invention, as defined by claim 19, a single address ("no more than one of the plurality of addresses") is used to establish more than one channel connection. Furthermore, the channel connections established through this single address

are associated with one specific port on each PHY ("first ports"). These features are not disclosed, taught, or suggested by *Delvaux* or by *Delattre et al.*

3) Conclusion

Accordingly, the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 19. Since the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claim 19, a *prima facie* case establishing an obviousness rejection by *Delvaux* in view of *Delattre et al.* has not been made. Thus, claim 19 is not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

d. Claims 33 and 40

Applicants respectfully traverse the rejection of claims 33 and 40, and submit that claims 33 and 40 are allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the feature of "where the ATM cell corresponds to the first class of service, providing the ATM cell to all of the first channel ports via a first unique address on the local interface."

*Delvaux* discloses an address expansion device for the UTOPIA bus, and describes both an ATM layer device and a plurality of physical layer devices (PHYs). Applicants will assume that *Delvaux* discloses switching ATM cells from the ATM layer device to a particular PHY based on a VPI/VCI value, although Applicants can find no specific discussion in *Delvaux* of this. Even so, *Delvaux* does not disclose providing an ATM cells to ***all*** first channel ports on a particular PHY when the cell corresponds to a first class of service, as recited in claims 33 and 40. Furthermore, *Delvaux* does not disclose providing the cell to all first channel ports "via a first unique address on the local interface," as recited in claims 33 and 40.

Nor does *Delattre et al.* disclose this feature. *Delattre et al.* discloses a shaper associated with by class of service. Applicants will assume, *arguendo*, that a shaper is dedicated to a port. Even so, *Delattre et al.* does not teach providing a cell having a particular class of service to ***all*** first channel ports on a PHY as recited in claims 33 and 40. Furthermore, *Delattre et al.* does not disclose providing the cell to all first channel ports "via a first unique address on the local interface," as recited in claims 33 and 40.

Accordingly, the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claims 33 and 40. Since the proposed combination of *Delvaux* in view of *Delattre et al.* does not teach at least the above-described features recited in claims 33 and 40, a *prima facie* case establishing an obviousness rejection by *Delvaux* in view of *Delattre et al.* has not been made. Thus, claims 33 and 40 is not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

e. Claims 9, 18, 26-32, and 47-60

Claims 9, 18, 26-32, and 47-60 are cancelled without prejudice, waiver, or disclaimer, and therefore, the rejection of these claims is rendered moot. Applicants take this action merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of these cancelled claims in a continuing application, if Applicants so choose, and do not intend to dedicate any of the cancelled subject matter to the public.

f. Claims 2-8, 11-17, 20-25, 34-39, 41-46, and 62-67

Since claims 1, 10, 19, 33, 40, and 61 are allowable, Applicants respectfully submit that claims 2-8, 11-17, 20-25, 34-39, 41-46, and 62-67 are allowable for at least the reason that each

depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d1596, 1598 (Fed. Cir. 1988). Therefore, Applicants respectfully request that the rejection of claims 2-8, 11-17, 20-25, 34-39, 41-46, and 62-67 be withdrawn.

3. Newly Added Claims

Applicant submits that no new matter has been added in new claims 68-90 and that new claims 68-90 are allowable over the cited references. Specifically, independent claim 68 is allowable for at least the reason that the cited references do not disclose, teach, or suggest at least the feature of "a local interface in communication with the ATM layer device and the plurality of physical layer devices, the local interface establishing a plurality of first class connections, each first class connection being between one of the ATM communications channels and one of the first channel ports, all of the first class connections using a single address on the local interface." Independent claim 76 is allowable for at least the reason that the cited references do not disclose, teach, or suggest at least the feature of "an asynchronous transfer mode (ATM) layer device...the ATM layer device being in communication with the address expansion device through the address expansion device's address on the local interface." Independent claim 84 is allowable for at least the reason that the cited references do not disclose, teach, or suggest "a communication means for interfacing the ATM layer means and the plurality of physical layer means, the communication means establishing a plurality of first class connections, each first class connection being between one of the ATM communications channels and one of the first channel ports, all of the first class connections using a single address on the local interface." Therefore, Applicants request that the Examiner enter and allow the above new claims.

## CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and presently pending claims 1-8, 10-17, 19-25, 33-46, and 61-90 be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

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